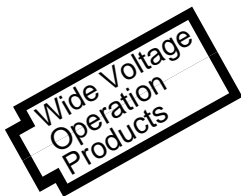


SED1181FLA/DLA

Dot Matrix Extension LCD Driver



- 64-bit High Voltage Output
- Display Duty Static to 1/32
- CMOS High-Voltage Process

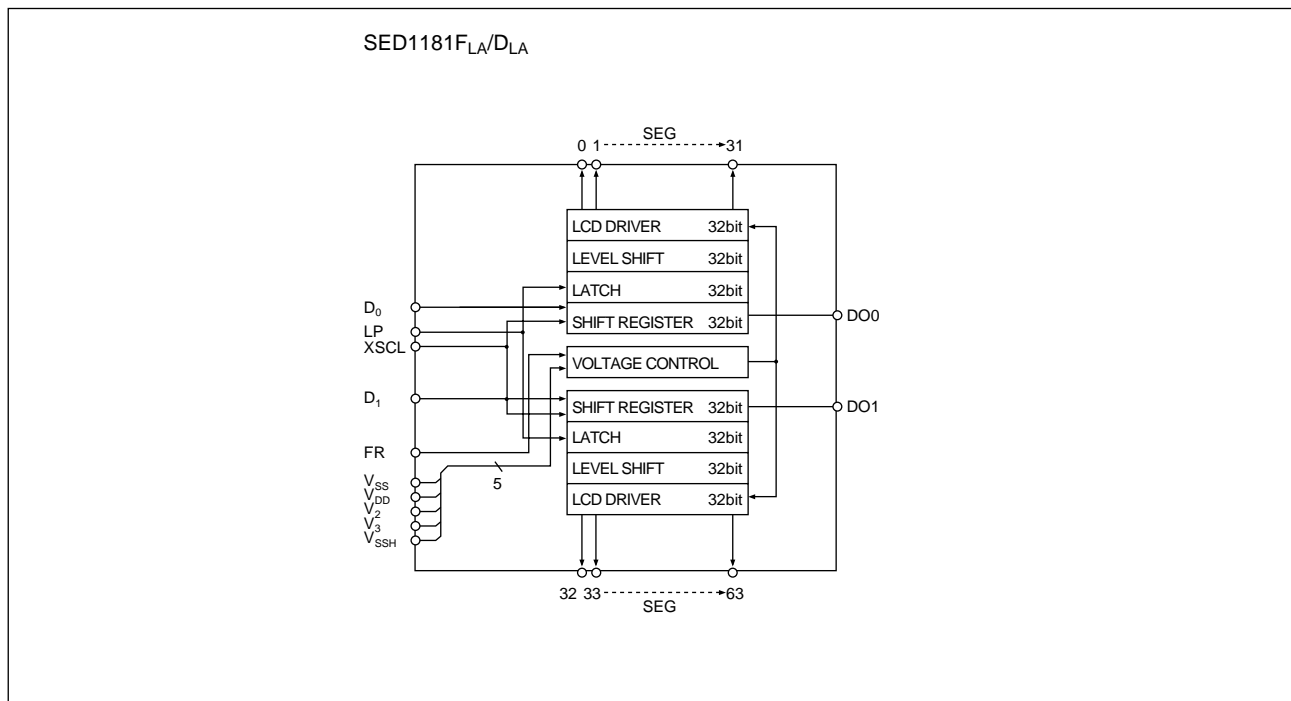
OVERVIEW

The SED1181FLA is a segment (column) driver capable of driving a high-contrast, low-capacity dot matrix LCD (Liquid Crystal Display) panel at a duty factor ranging from static to 1/32 duty. It is ideally suited as a display extension for the SED1210F, SED1278F, or four-bit microcomputers.

FEATURES

- Display duty factor Static to 1/32
- 64-bit high voltage output LCD driver (dedicated segment driver).
- The forward shift construction facilitates mounting of the 1/32-duty panel.
- Capable of a serial cascade connection.
- Power supply for logic operations -2.4 to -6.0V
- Independent transmission of higher-/lower-order serial data.
- Package SED1181FLA: QFP5-80pin (plastic),
SED1181DLA: Die form (Al pad)

BLOCK DIAGRAM



SED1181FLA/DLA

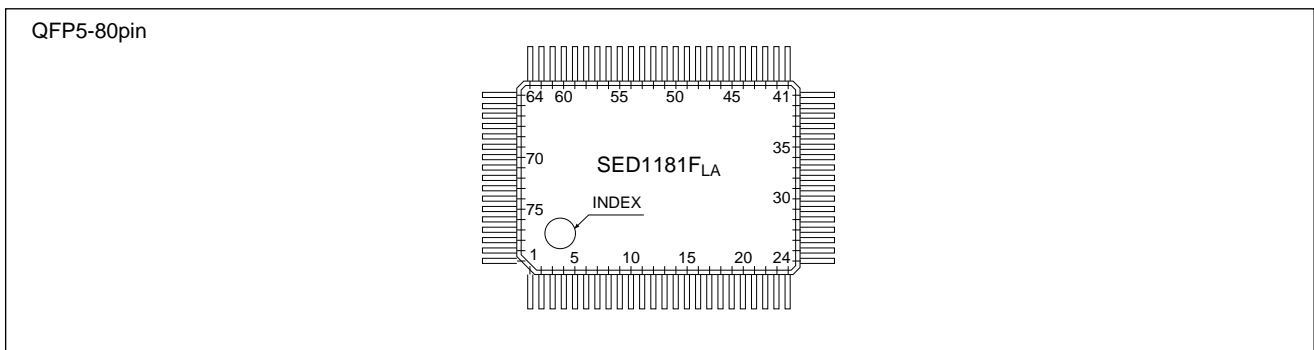
PIN DESCRIPTION

Pin Name	I/O	Function	Qty.
SEG 0-63*	O	Segment output for driving the LCD (X side) The output changes at the falling edge of the LP latch pulse.	64
XSCL	I	Shift clock for the display data. At its falling edge, serial display data of D0 or D1 is input.	1
LP	I	Latch pulse for the display data. Latching occurs at the falling edge.	1
FR	I	Frame (AC-conversion) signal for the LCD drive waveforms.	1
DO0	O	Outputs (the input serial display data from D0.)	1
DO1	O	Outputs (the input serial display data from D1.)	1
DO, D1	I	Inputs two series of serial display data (input occurs at the falling edge of XSCL)	2
V _{DD} , V _{SS}	I	Power supply for logic. V _{DD} : (V _{CC} >, V _{SS} : (GND).	2
V ₂ , V ₃ , V _{SS-1}	I	Power supply for driving the LCD. V _{DD} >V ₂ >V ₃ >V _{SS-1}	3

* D0 serial display data → SEG0 to SEG31 display data.

* D1 serial display data → SEG32 to SEG63 display data.

PIN CONFIGURATION



No.	Name	No.	Name	No.	Name	No.	Name
1	SEG27	21	SEG7	41	SEG36	61	SEG56
2	SEG26	22	SEG6	42	SEG37	62	SEG57
3	SEG25	23	SEG5	43	SEG38	63	SEG58
4	SEG24	24	SEG4	44	SEG39	64	SEG59
5	SEG23	25	SEG3	45	SEG40	65	SEG60
6	SEG22	26	SEG2	46	SEG41	66	SEG61
7	SEG21	27	SEG1	47	SEG42	67	SEG62
8	SEG20	28	SEG0	48	SEG43	68	SEG63
9	SEG19	29	DO0	49	SEG44	69	V _{SSH}
10	SEG18	30	NC	50	SEG45	70	V ₂
11	SEG17	31	NC	51	SEG46	71	V ₃
12	SEG16	32	DI	52	SEG47	72	V _{SS}
13	SEG15	33	D0	53	SEG48	73	V _{DD}
14	SEG14	34	XSCL	54	SEG49	74	DO1
15	SEG13	35	LP	55	SEG50	75	NC
16	SEG12	36	FR	56	SEG51	76	NC
17	SEG11	37	SEG32	57	SEG52	77	SEG31
18	SEG10	38	SEG33	58	SEG53	78	SEG30
19	SEG9	39	SEG34	59	SEG54	79	SEG29
20	SEG8	40	SEG35	60	SEG55	80	SEG28

■ ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage (1)	V_{SS}	-7.0 to 0.3	V
Supply voltage (2)	V_{SSH}	-7.0 to 0.3	V
	V_2, V_3		
Input voltage	V_{IN}	$V_{SS}-0.3$ to 0.3	V
Operating temperature	T_{opr}	-3.0 to 85	°C
Storage temperature	T_{stg}	-65 to 150	°C
Solder temperature/time	T_{sol}	260°C, 10s (at lead)	—

■ ELECTRICAL CHARACTERISTICS

($T_a = -30$ to 85°C (unless otherwise specified))

($V_{SS} = -5.0\text{V} \pm 10\%$ (unless otherwise specified))

● DC Characteristics

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	
Supply voltage (1)	V_{SS}		-6.0	-5.0	-2.4	V	
Supply voltage (2)	V_2		V_{SSH}	—	V_{DD}	V	
	V_3		V_{SSH}	—	V_{DD}	V	
	V_{SSH}	Recommended operation V_{SSH}	-12.0	—	-3.0	V	
		Potential operation V_{SSH}^{*2}	-12.0	—	-2.5	V	
HIGH input voltage	V_{IH}		$0.2V_{SS}$	—	$V_{DD}+0.3$	V	
LOW input voltage	V_{IL}		$V_{SS}-0.3$	—	$0.8V_{SS}$	V	
HIGH output voltage	V_{OH}	$I_{OH} = -0.6\text{mA}$	-0.4	—	—	V	
LOW output voltage	V_{OL}	$I_{OL} = 0.6\text{mA}$	—	—	$V_{SS}+0.4$	V	
Input leak current	I_{LI}	$0\text{V} \leq V_{IN} \leq V_{SS}$	—	0.05	2.0	μA	
Output leak current	I_{LO}	$0\text{V} \leq V_{OUT} \leq V_{SS}$	—	0.05	5.0	μA	
Transmission clock	XSCL		—	—	600	KHz	
Frame cycle	FR		—	1/60	—	sec	
Input terminal capacity	C_{IN}	$T_a = 25^\circ\text{C}$	—	5.0	8.0	pF	
SEG. output ON resistance	R_{SEG}	$ \Delta V_{ON} 0.1\text{V}$ $T_a = 25^\circ\text{C}$	V_{SSH}	-8.0V	—	3.0	—
				-5.0V	—	5.0	—
				-3.0V	—	16.0	—
Static current consumption	I_Q	$V_{SSH} = -12.0\text{V}, V_{SS} = -6.0\text{V},$ $V_{IN} = V_{DD}$	—	0.05	30.0	μA	
Logic power supply's average current consumption	$I_{SS OP}$	$V_{SS} = -5.0\text{V}, V_{IH} = V_{DD}, V_{IL} = V_{SS}$ FR cycle = 16.7ms (50% duty) LP cycle = 520 μs XSCL = 400KHz (duty 50%) All data input: Inverted at each bit All output terminals are open.	—	250	300	μA	
LCD's average current consumption	I_{SSHOP}	$V_{SS} = -4.5\text{V}, V_2 = -4.8\text{V}$ $V_3 = -7.2\text{V}, V_{SSH} = -12.0\text{V}$ Other conditions are identical to those for $I_{SS OP}$.		8	10	μA	

*1 The voltage values are based on the $V_{DD}=0\text{V}$ reference voltage.

*2 The potential operation V_{SSH} refers to the range in which operation is functionally possible, although its drive output ON resistance will be higher than that of the recommended operation V_{SSH} . It is advisable to determine whether or not to use drivers on the basis of an experimental confirmation based on the operation of the LCD panel to actually be used.

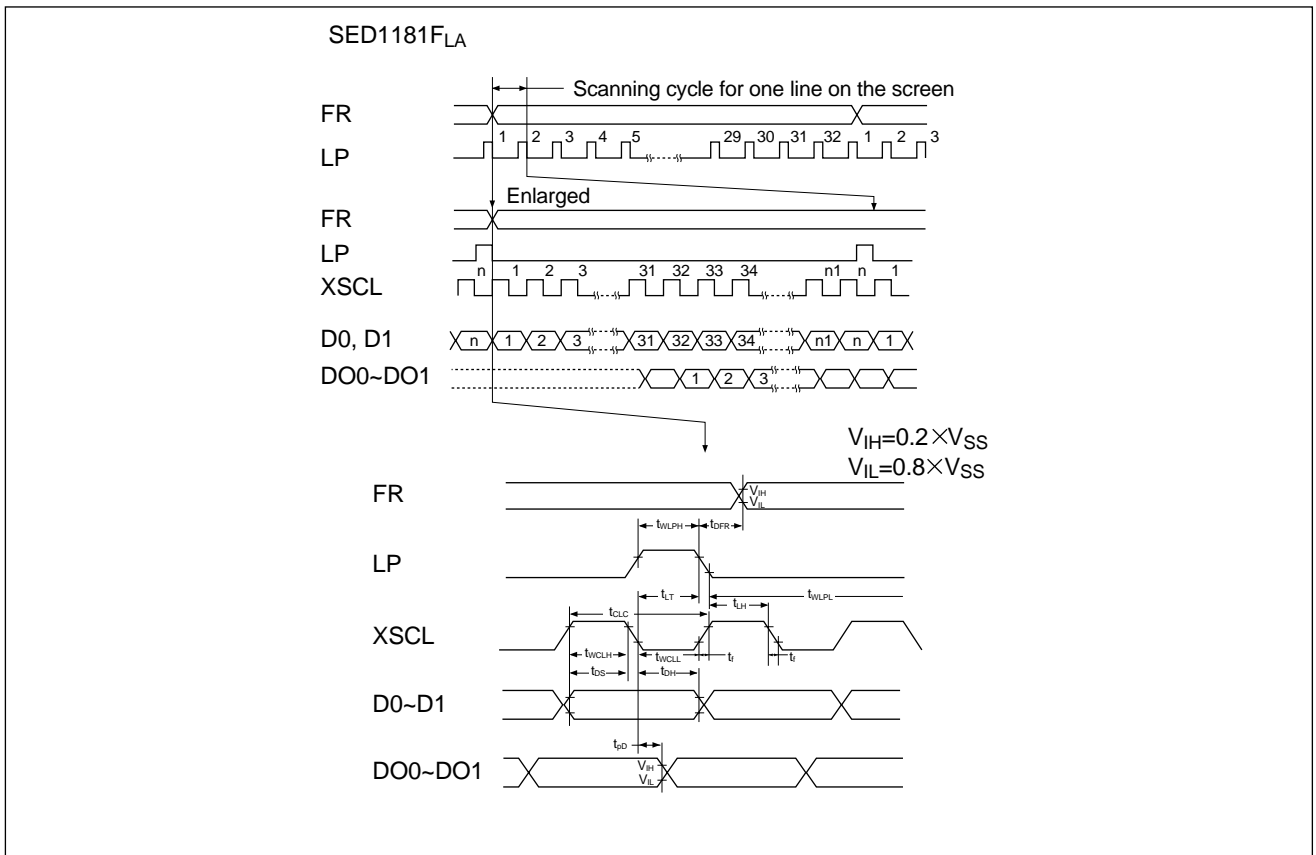
SED1181FLA/DLA

● AC Characteristics

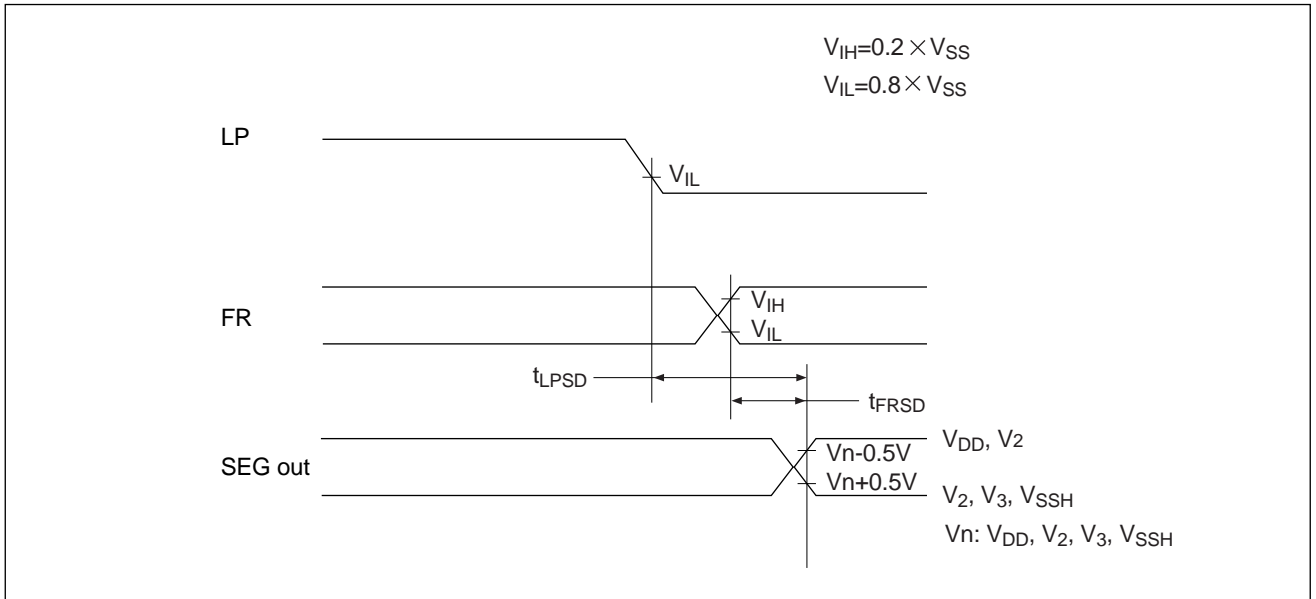
(Ta = -30 to 85°C, V_{SS} = -6.0V to 2.4V)

Characteristic	Signal	Condition	Min.	Typ.	Max.	Unit
Shift clock cycle	t _{CLC}		1.66	—	—	μs
Shift clock pulse width (High)	t _{WCLH}		450	—	—	ns
Shift clock pulse width (Low)	t _{WCLL}		600	—	—	ns
Data set-up time	t _{DS}		100	—	—	ns
Data hold time	t _{DH}		30	—	—	ns
Latch pulse width (High)	t _{WLPH}		200	—	—	ns
Latch pulse width (Low)	t _{WLPL}		600	—	—	ns
Latch timing cycle	t _{LT}		200	—	—	ns
Latch hold time	t _{LH}		100	—	—	ns
Permitted Frame signal delay time	t _{DFR}		-500	0	500	ns
Input signal rising time	t _r		—	—	50	ns
Input signal falling time	t _f		—	—	50	ns
Serial data output delay time	t _{PD}		20	—	250	ns

● Timing Chart



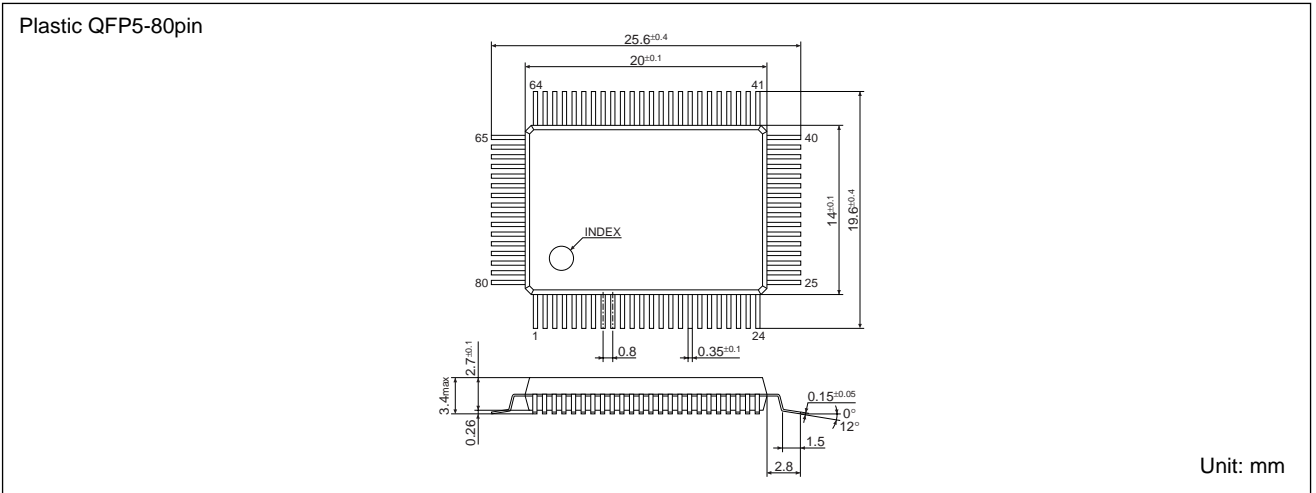
● Characteristics of SEG. Output Signal Timing



($T_a = -30$ to 85°C , $V_{SS} = -6.0\text{V}$ to -2.4V)

Characteristic	Signal	Condition	Min.	Typ.	Max.	Unit.
LP-SEG output delay time	t_{LPSD}	$V_{SSH} = -3.0\text{V}$ to -12.0V $CL = 100\text{pF}$	—	—	4.5	μs
FR-SEG output delay time	t_{FRSD}		—	—	4.5	μs

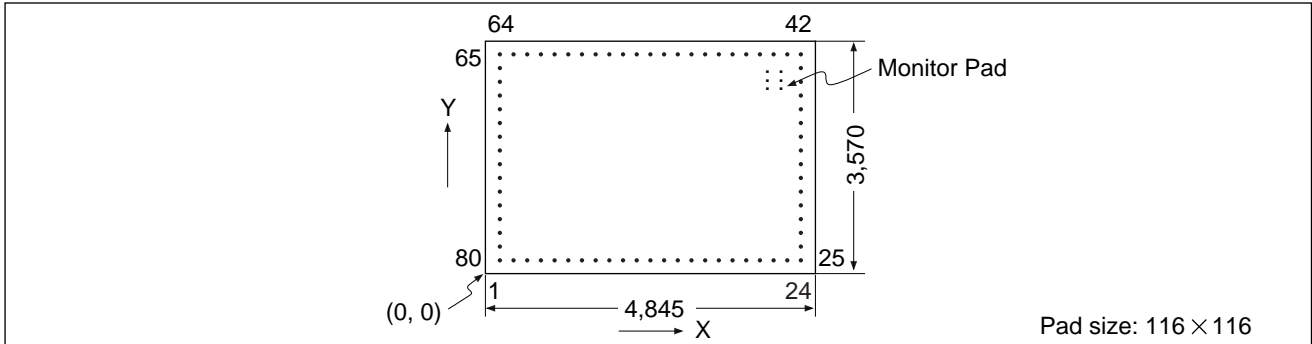
■ PACKAGE DIMENSIONS



SED1181FLA/DLA

SED1181DLA

● PAD LAYOUT

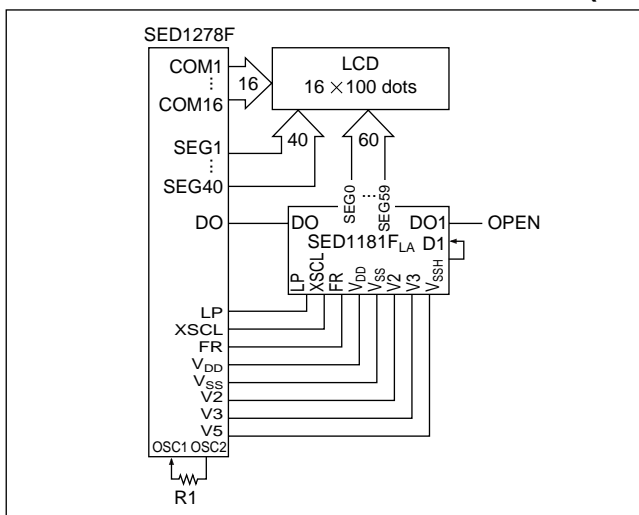


● PAD COORDINATION

Unit: μm

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	SEG27	155	155	28	SEG0	4,690	916	55	SEG50	1,947	3,415
2	SEG26	423		29	DO0		1,107	56	SEG51	1,756	
3	SEG25	614		30	NC		1,297	57	SEG52	1,566	
4	SEG24	804		31	NC		1,488	58	SEG53	1,375	
5	SEG23	995		32	D1		1,678	59	SEG54	1,185	
6	SEG22	1,185		33	D0		1,868	60	SEG55	995	
7	SEG21	1,375		34	XSCL		2,059	61	SEG56	804	
8	SEG20	1,566		35	LP		2,249	62	SEG57	614	
9	SEG19	1,756		36	FR		2,440	63	SEG58	423	
10	SEG18	1,947		37	SEG32		2,630	64	SEG59	155	3,392
11	SEG17	2,137		38	SEG33		2,820	65	SEG60		3,201
12	SEG16	2,327		39	SEG34		3,011	66	SEG61		3,011
13	SEG15	2,518		40	SEG35		3,201	67	SEG62		2,820
14	SEG14	2,708		41	SEG36		3,392	68	SEG63		2,630
15	SEG13	2,899		42	SEG37	4,422	3,415	69	VSSH		2,440
16	SEG12	3,089		43	SEG38	4,231		70	V ₂		2,249
17	SEG11	3,279		44	SEG39	4,041		71	V ₃		2,059
18	SEG10	3,470		45	SEG40	3,851		72	V _{SS}		1,868
19	SEG9	3,660		46	SEG41	3,660		73	V _{DD}		1,678
20	SEG8	3,851		47	SEG42	3,470		74	DO1		1,488
21	SEG7	4,041		48	SEG43	3,279		75	NC		1,297
22	SEG6	4,231		49	SEG44	3,089		76	NC		1,107
23	SEG5	4,422	345	50	SEG45	2,899		77	SEG31		916
24	SEG4	4,690	536	51	SEG46	2,708		78	SEG30		726
25	SEG3		726	52	SEG47	2,518		79	SEG29		536
26	SEG2			53	SEG48	2,327		80	SEG28		345
27	SEG1			54	SEG49	2,137					

■ LCD PANEL CONNECTION EXAMPLE (for a 20 character \times 2 row display)



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