深圳市希恩凯电子有限公司

SHENZHEN CNK ELECTRONIC CO.,LTD.

Specification

TFT-LCD module

Module(型号)：	CNKT0280-11004A
Customer（客户）：	
Customer P/N（客户型号）：	

If there is no special request from customer, SHENZHEN C N K ELECTRONIC CO., LTD will not reserve the tooling of the product under the following conditions:
1.There is no response from customer in one years after SHENZHEN C N K ELECTRONIC CO., LTD submit The samples;
2.There is no order in one years after the latest mass production.And correlated data (include quality record) will be reserved one year more after tooling was discarded.

Approved by（批准）：	
Qualified（合格）：	Unqualified（不合格）：

PREPARED	CHECKED	APPROVED

SHENZHEN CNK ELECTRONIC CO.,LTD

REVISION RECORD

REV NO	REV DATE	CONTENTS	REMARKS
1.0	2010-7-22	First Release	

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1.0 General Specifications

CNKT0280-11004A ***is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It iscomposed of a color TFT-LCD panel, driver IC, FPC and a back light unit. The module display area contains 240x 320pixels and can display up to 262K colors. This product accords with RoHS environmentalcriterion.***

Item	Contents	Unit
LCD Type	TFT TRANSMISSIVE	/
Viewing direction	12:00	O' Clock
Module outline (W x HxD)	50X69.2X2.25	mm
Active area (WxH)	43.2X57.6	mm
Number of Dots	240(RGB) x320	/
Driver IC	ILI9341	/
Colors	262K	/
Backlight Type	LED	/
Interface Type	System parallel interface	/
Input voltage	2.8	V

2.0 ABSOLUTE MAXIMUM RATINGS

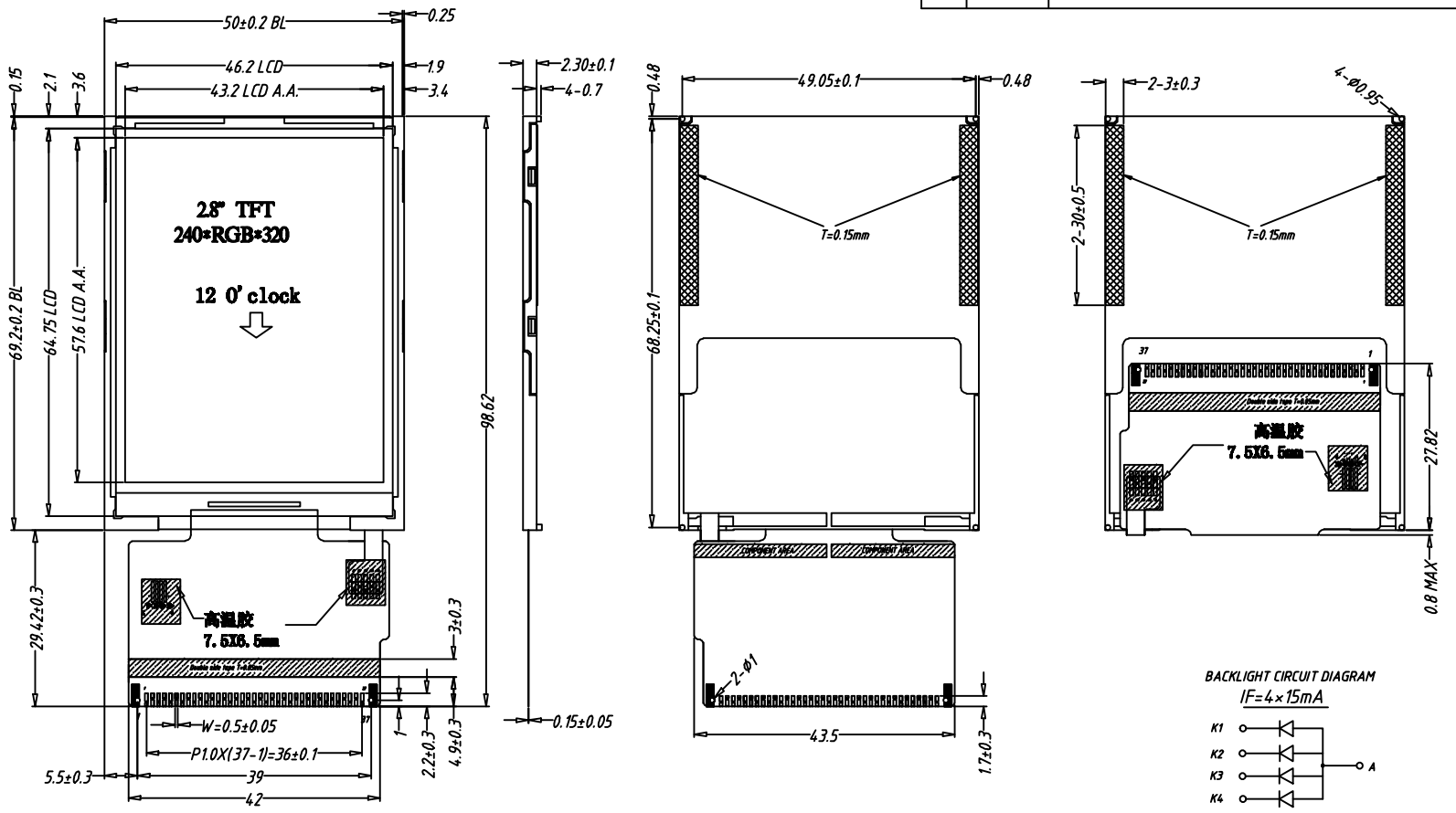
Parameter	*Symbol*	*Min*	*Max*	*Unit*
Input voltage	Vin	*-0.3*	*VCC+ 0.3*	**V**
Operating temperatur	Top	*-20*	*70*	℃
Storage temperature	Tst	*-30*	*80*	℃

3.0 ELECTRICAL CHARACTERISTICS

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Supply voltage for logic	Vcc -Vss	*2.6*	*2.8*	*3.3*	V
Input Current	Idd	-	-	*4.0*	mA
Input voltage ' H ' level	Vih	*0.8 Vdd*	--	*Vdd*	V
Input voltage ' L ' level	Vil	*Vss*	*0*	*0.2 Vcc*	V
Output voltage ' H ' level	Voh	*0.8 Vdd*	--	*Vdd*	V
Output voltage ' L ' level	Vol	*Vss*	*0*	*0.2 Vcc*	V

5.0 DIMENSIONAL DRAWING

版本	变更日期	变更内容	核 准



PIN	SYMBOL
1	DB0
2	DB1
3	DB2
4	DB3
5	GND
6	IOVCC
7	/CS
8	RS
9	WR
10	RD
11	NC
12	X+
13	Y+
14	X-
15	Y-
16	A
17	K1
18	K2
19	K3
20	K4
21	NC
22	DB4
23	DB8
24	DB9
25	DB10
26	DB11
27	DB12
28	DB13
29	DB14
30	DB15
31	RESET
32	VCC
33	IOVCC
34	GND
35	DB5
36	DB6
37	DB7

1.DISPLAY TYPE	2.8" TFT,TRANSMISIVE
2.VIEWING DIRECTION	12 O'CLOCK
3.DRIVER IC	IL19341
4.BACKLIGHT	4 Chip-White LED,Parallel
5.OPERATIVE VOLTAGE	2.8V
6.OPERATIVE TEMP.	-10°C TO 60°C
7.STORAGE TEMP.	-20°C TO 70°C
8.CONNECTOR	FPC

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Dwg.No	CNKT0280-11004A

Tolerance	±0.2
Unit	mm
Scale	
Date	2011/11/8
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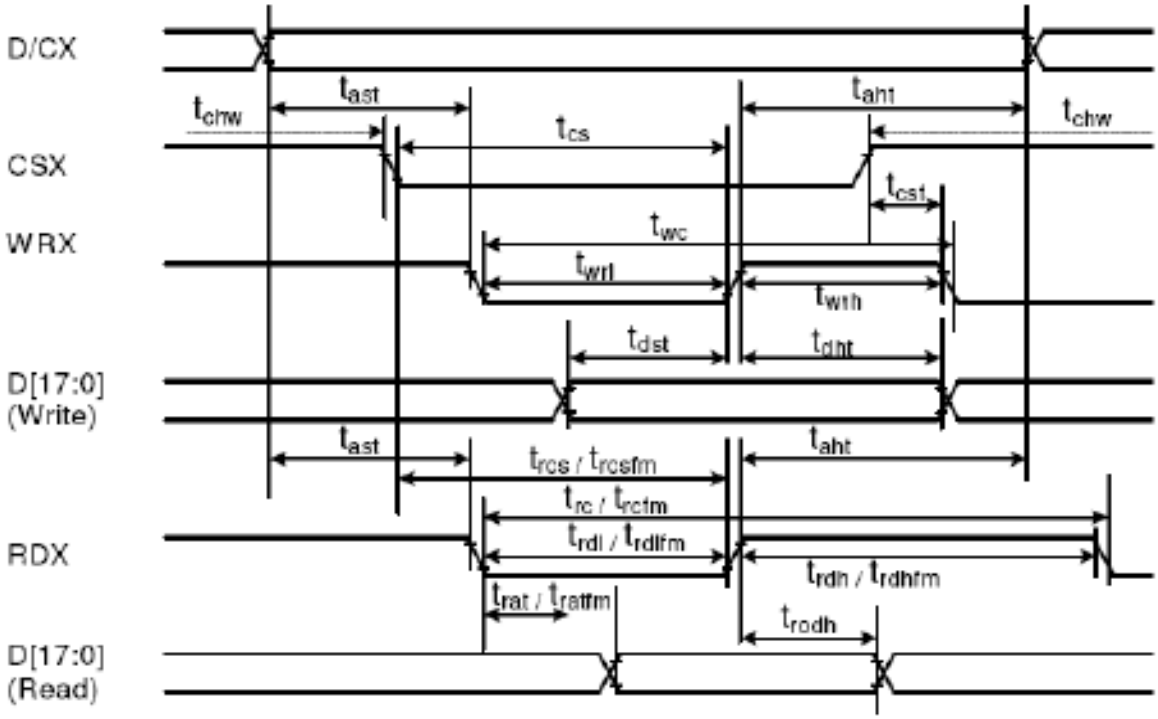
6.0 INTERFACE PIN CONNECTIONS

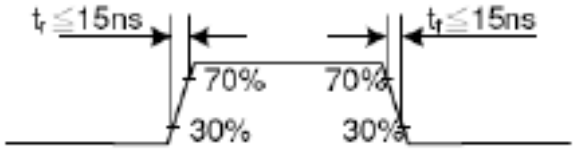
No	Name	Description
1–4	DB0—DB3	Bidirectional Data Bus lines
5	GND	Ground
6	IOVCC	Power supply for I/O logic (1.8V or 2.8V)
7	/CS	Chip select signal
8	RS	Select data or command, L:Command,H:D
9	WR	Write enable signal
10	RD	Read enable signal
11	LCD_ID	NC
12	XR	NO connection
13	YU	NO connection
14	XL	NO connection
15	YD	NO connection
16	LED-A	Backlight , Anode
17	LED-K1	Backlight , Cathode1
18	LED-K2	Backlight , Cathode2
19	LED-K3	Backlight , Cathode3
20	LED-K4	Backlight , Cathode4
21	NC/FMARK	NC
22	DB4	Bidirectional Data Bus lines
23–30	DB8—DB15	Bidirectional Data Bus lines
31	/RESET	Reset signal pin,
32	VCI	Power supply for analog (2.8V)
33	VCC	Power supply for analog (2.8V)
34	GND	Ground
35–37	DB5—DB7	Bidirectional Data Bus lines

6.1TIMING CHARACTERISTICS

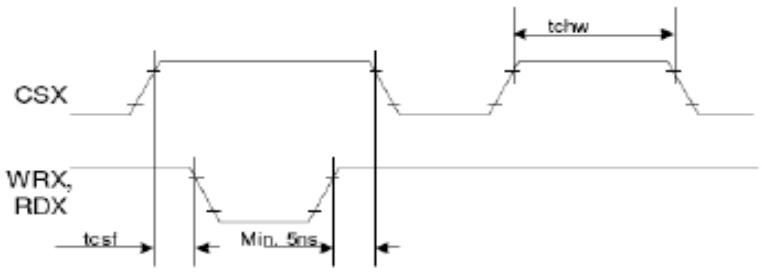


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

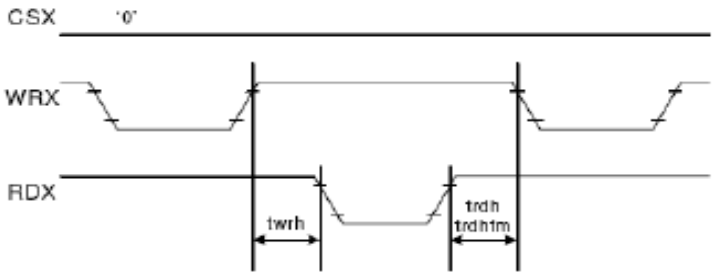


CSX timings :



Note: Logic high and low levels are specified as 90% and 70% of VDDI for Input signals.

Write to read or read to write timings:



Note: Logic high and low levels are specified as 90% and 70% of VDDI for Input signals.

6.3 BLOCK DIAGRAM OF LCM